

CLAIMS

What is claimed is:

1. A method for implementing skip over redundancy decode on a chip, comprising the steps of:

implementing a decode circuit for redundant decode on a chip by providing for said decode circuit a decoder and a separate carry function for said decode circuit.

2. The method according to claim 1, wherein the separate carry function is implemented separately from the decoder and implemented with carry logic.

3. The method according to claim 2 wherein said decoder of said decoder circuit is partitioned into even decode and odd decode logic components.

4. The method according to claim 3 wherein the even decode and odd decode logic components have an output wire track and the physical partitioning and arrangement of said even decode and odd decode logic components and their outputs share a common wire track.

5. The method according to claim 3 wherein the even decode and odd decode logic components have an output wire track and the physical partitioning and arrangement of said even decode and odd decode logic components and their outputs share a common wire track approaching said carry logic from opposition directions.

6. The method according to claim 3 wherein the physical partitioning and arrangement of said even decode and odd decode logic and the associated carry logic performing the carry function for said decode circuit are placed laid out in placement into unused “whitespace” within a chip macro, and thus by said placement save chip area.

7. The method according to claim 6 wherein the even decode and odd decode logic components have an output wire track and the physical partitioning and arrangement of said even decode and odd decode logic components and their outputs share a common wire track approaching said carry logic from opposite directions.
8. The method according to claim 5 wherein said common wiring track decreases the wiring tracks (required to implement the decoder circuit).
9. The method according to claim 8 wherein said sharing of a common wiring track increases the wiring tracks (resources) available to a next level of chip assembly.
10. The method according to claim 9 wherein said decode circuit is used to implement I/O redundancy control logic and provides one wire trace for two I/Os.

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